AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented): A method for storing register properties of a hardware device having heterogeneous memory in a data-structure, said hardware device being built according to a structure of modules and dependent sub-modules, wherein said register properties correspond to register properties of said modules and said dependent sub-modules, wherein said method comprises:

storing said register properties in a data-structure according to said structure of said hardware device; and

arranging said register properties in an array for each module or dependent sub-module.

2. (previously presented): A storage device comprising a data structure,

wherein said data structure comprises register properties of a hardware device having heterogeneous memory, said hardware device having a structure of modules and dependent sub-modules, wherein said register properties correspond to register properties of said modules and said dependent sub-modules, wherein said data structure holds said register properties in a structure according to said structure of said hardware device, and wherein said register properties are arranged in an array for each module or dependent sub-module.

3. (previously presented): The storage device according to claim 2, wherein said array corresponding to a module of said hardware device comprises a number of repetitions indicator, adapted to indicate the number of reoccurrences of a submodule of said module.

4. (previously presented): The storage device according to claim 2, wherein said register properties in each array includes either one of an initial value of a register, the read-write bits, unstable read-write bits or read-reset bits.

5. (canceled).

6. (previously presented): The storage device according to claim 2, wherein said data structure is used in an access test executed by a generic test device.

7. (currently amended): The storage device according to claim 6, wherein said access tests of ~~said~~ an ASIC includes either one of Read/Write of multiple patterns to two registers, data-bus test, address-bus test, device reset test or test initial values of all registers.

8. (new): The method according to claim 1, wherein said array corresponding to a module of said hardware device comprises a number of repetitions indicator, adapted to indicate the number of reoccurrences of a submodule of said module.

9. (new): The method according to claim 1, wherein said register properties in each array includes either one of an initial value of a register, the read-write bits, unstable read-write bits or read-reset bits.

10. (new): The method according to claim 1, wherein said data structure is used in an access test executed by a generic test device.

11. (new): The method according to claim 10, wherein said access test of an ASIC includes either one of Read/Write of multiple patterns to two registers, data-bus test, address-bus test, device reset test or test initial values of all registers